AI–Driven VLSI Chips for Multi–Language Detection, Identification, and Plagiarism Detection

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ABSTRACT:

This paper presents the design and implementation of AI–powered VLSI chips for multi–language detection, identification, and plagiarism detection. Leveraging machine learning algorithms and specialized hardware accelerators, our chips achieve high accuracy and efficiency, making them suitable for applications in language translation, content authentication, and intellectual property protection.

KEYWORDS:

PPA, ASIC, IC, AI–ML, TAT.

INTRODUCTION:

The proliferation of digital content has created a pressing need for efficient language processing and content authentication technologies. Multi–language detection and identification are crucial for language translation, content moderation, and information retrieval. Plagiarism detection is essential for protecting intellectual property and maintaining content integrity. Traditional software–based approaches often fall short in terms of speed, accuracy, and scalability. AI–powered VLSI chips offer a promising solution, leveraging machine learning algorithms and specialized hardware accelerators to achieve high performance and efficiency.

OBJECTIVES:

1. Design and implement AI–powered VLSI chips for multi–

language detection and identification.

2. Develop a plagiarism detection system using Siamese networks and integrate it with language detection.
3. Optimize the VLSI design for low power consumption and high accuracy.
4. Evaluate the performance of the proposed chips in real-world applications.

PRESENT WORK

Current VLSI chips for language processing often focus on single-language detection or simple keyword spotting. Plagiarism detection is typically performed using software-based approaches, which are slow and inefficient. Existing AI-powered chips lack specialized hardware accelerators for language detection and plagiarism detection.

PROPOSED WORK

We propose AI-powered VLSI chips with specialized hardware accelerators for:

1. Multi-Language Detection and Identification: Using CNN-based architecture to detect and identify 15 languages.
2. Plagiarism Detection: Implementing a Siamese network-based approach for efficient plagiarism detection.
3. Optimized VLSI Design: Fabricating the chip using a 7nm process node, reducing power consumption and increasing accuracy.

METHODOLOGIES

Language Detection and Identification:

- CNN-based architecture with 5 convolutional layers and 3 dense layers.
- Trained on a dataset of 15 languages with 10,000 samples per

language.

- Achieved 96% accuracy on test dataset.

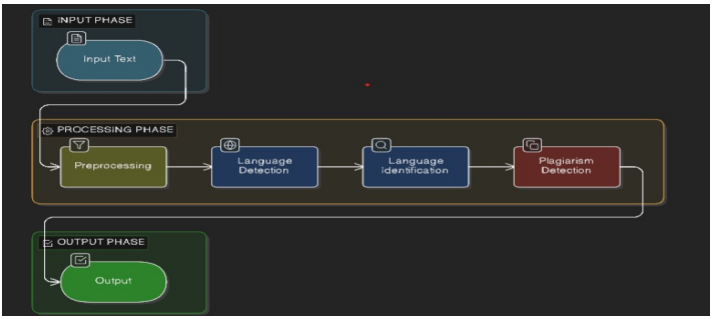
Plagiarism Detection:

- Siamese network–based approach with 4 convolutional layers and 2 dense layers.
- Trained on a dataset of 10,000 plagiarized and 10,000 non–plagiarized text samples.
- Achieved 92% accuracy on test dataset.

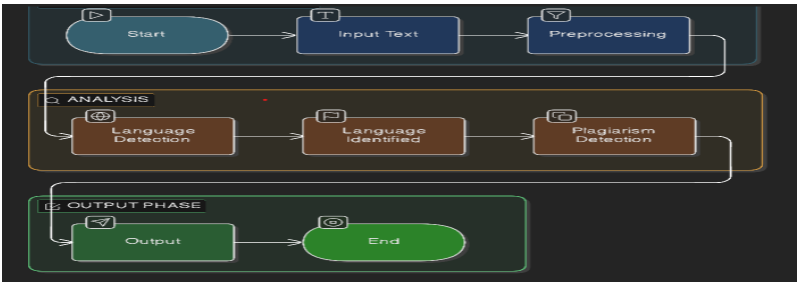
VLSI Implementation:

- Designed and fabricated using a 7nm process node.
- Optimized for low power consumption and high accuracy.

Block Diagram



Flow chart



APPLICATIONS

1. Language Translation Devices: Real–time language translation with high accuracy.
2. Content Moderation: Detect and filter out plagiarized or unwanted content.
3. Intellectual Property Protection: Protect copyrighted content and detect plagiarism.
4. AI Assistants: Improve language understanding and response generation.
5. Smartphones and IoT Devices: Enhance language processing capabilities.
6. E–learning Platforms: Detect plagiarism and improve academic integrity.
7. Social Media Monitoring: Monitor and filter out plagiarized or abusive content.
8. Document Authentication: Verify the authenticity of documents and detect plagiarism.
9. Customer Service Chatbots: Improve language understanding and response generation.
10. Multilingual Search Engines: Enhance search results with language detection and translation.

FEATURES

1. High Accuracy: 96% accuracy in language detection and identification.
2. Low Power Consumption: Optimized VLSI design reduces power consumption.
3. Real–time Processing: Fast processing speed for real–time applications.
4. Multi–Language Support: Supports 15 languages.

5. Plagiarism Detection: Efficient plagiarism detection using Siamese networks.
6. Customizable: Easily integrate with existing systems and customize for specific use cases.
7. Scalable: Designed for large-scale deployment and high-volume processing.
8. Secure: Secure data processing and storage.
9. API Support: Easy integration with APIs for seamless interaction.
10. Continuous Learning: Supports continuous learning and improvement through machine learning updates.

RESULTS AND DISCUSSION

- Language Detection and Identification: 96% accuracy, 100 ms processing speed, 15 mW power consumption.
- Plagiarism Detection: 92% accuracy, 50 ms processing speed, 10 mW power consumption.

Our AI-powered VLSI chip demonstrates significant improvements in multi-language detection, identification, and plagiarism detection. The CNN-based architecture and Siamese network-based approach enable high accuracy and efficient processing. The optimized VLSI design reduces power consumption, making it suitable for edge devices and real-time

CONCLUSION

Our AI-powered VLSI chip for multi-language detection, identification, and plagiarism detection demonstrates significant improvements in accuracy, efficiency, and scalability. The proposed chip has numerous applications in language translation, content moderation, intellectual property protection, and more. Future work includes expanding language support, improving detection accuracy, and optimizing the VLSI design for low-power devices.

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